IN THE SPECIFICATION:

Please replace the third full paragraph of specification page 2 with the following replacement paragraph:

None of these above conditions will produce an indeterminate output from the present invention and~~. While~~ while under normal operation, the failsafe bias will not affect the receiver performance from both speed (bandwidth) ~~and or~~ and/or a jitter/noise point of view.

Please replace the second full paragraph of specification page 4 with the following replacement paragraph:

FIG. 1A shows a diagram of a preferred embodiment of the present invention. An input signal, Vin controls and selects output current signals Ip and Im that are driven 10 into a transmission line 12. The driver 10 is a current driver with a high output impedance. In practice there may be a single twisted pair or two transmission lines, but as discussed below since Ip and Im are not equal, there will be a return current [~~is~~] that is absorbed by the current sense amplifier when a twisted pair is used or that travels through a shield if present. Transmission lines are not fundamental to the practical use of the present invention, but if not used some noise friendly path must be provided for the return current Is. In one logic state Ip is a positive current out into a first transmission line 50 and Im is a negative current in from a second transmission line 52. In the opposite logic state Ip is a negative current from the first transmission line 50 and Im is a positive current into the second transmission line 52. In another preferred embodiment it is possible to have current driven only into one transmission line.

Please replace the first full paragraph of specification page 6 with the following replacement paragraph:

FIG. 1B illustrates the present invention's toleration of current noise. Generally, a portion of Ip and Im, i1 and i2, travels through to the differential current sense circuit 54. The current sense 54 designed with a differential current threshold Ith that must be reached in order for the valid logic signal to be recognized. So the differential between Ip and Im must result in a differential between i1 and i2 that equals (or is greater than) the threshold Ith. In general, expressions, 13 and 15, respectively, for i1 and i2 are shown as functions of Ip and Im. If i2 is subtracted from i1, the result is shown in item 17. Since i1 – i2 must equal or exceed Ith, 19, the expression for Ith as a function of Ip and Im is shown in item 21. Evident from inspection is that Ip – Im must be large enough to ensure that i1-i2 exceeds the threshold. Under normal failsafe conditions, if the difference between I_p and I_m is not big enough, the difference between *a* and *b* (current distribution coefficients) is also small, which makes the equation of 21 very difficult to hold. In real application, it means that the receiver will be very robust against noise once it enters failsafe mode. It is evident from 21, that common mode current noise will cancel each other making this embodiment robust against common mode current noise. In a preferred embodiment, the present invention will tolerate 100uA of differential current noise. Other embodiments can be designed with greater noise immunity. Please note that i1 and i2 are both positive but of unequal values. If they were equal, there would be no difference when a logic level change occurs. These currents are usually not equal to each other except when the ~~line~~ lines short together. Under such conditions, the receiver will maintain the stable output with internal failsafe bias transistors P_{fl} and N_{fl} in figure 4. This offset provides the fails safe action of the present invention, but, in a preferred embodiment, only about 20uA of offset current generates very little additional power consumption, and embodiment of the present invention use virtually no extra die area.

Please replace the first full paragraph of specification page 7 with the following replacement paragraph:

FIG. 3 is a schematic of a current sensing circuitry consistent with a preferred embodiment of the present invention. Here two diode connected NMOS transistors, N3 and N4, are biased to siphon off I3 and I4, respectively, from currents in the transmission lines. N3 and N4 may be biased (not shown) along the diode-like curve to overcome any threshold and to present an impedance substantially greater than Rt to minimally affect the termination of the transmission lines. In one preferred embodiment N3 and N4 exhibit about 1 K ohms each, although other impedances can be used as known in the art. If N3 and N4 present about 2 K ohms across an equivalent 100 ohm transmission line, the Rt can be made equal to 105 ohms or appropriately higher or lower to maintain proper transmission line termination. However, as is known in the art, there is likely to be some harmless ringing due to some impedance mismatch even if care is taken to keep the diode transistors at a high impedance state. For example if Rt is 105 ohms across a 100 ohm transmission line, and the diode connected transistors present, for some processing reason, [a] very high impedances, the 5 ohm mismatch will only result in a reflection coefficient of about less than 2.5 percent.